EXPRESS MAIL MAILING [redacted]L
NUMBER: EI859862909US
DATE OF DEPOSIT: June 20, 2001

I hereby certify that this paper or fee is being
Deposited with the United States Postal Service
Under 37 C.F.R. 1.10 on the date indicated above
And is addressed to the Assistant Commissioner for
Patents, Washington, DC 20231

THORP REED AND ARMSTRONG, LLP
One Oxford Centre
301 Grant Street, 14th Floor
Pittsburgh, PA 15219-1425

Michelle M. Kalohelis

PATENT
Attorney Docket No.: DB000575-012

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Keeth, et al.	**Examiner:**	Not yet assigned
Serial No.:	Not yet assigned	**Art Unit:**	Not yet assigned
Filed:	20 June 2001		

Entitled: 256 MEG DYNAMIC RANDOM ACCESS MEMORY

PRELIMINARY AMENDMENT

Preliminary to the examination of the above-identified application filed herewith, please amend that application as follows.

In the Specification

Page 1, line 2, after the title, insert -- This Application is a divisional application of U. S. Application Serial No. 09/620,606 filed July 20, 2000, which is a divisional application of U.S. Application Serial No. 08/916,692 filed August 22, 1997.--

Page 52, line 18, delete "nine microfiche having a total of fifty-two frames" and substitute therefore --eleven microfiche having a total of sixty-six frames--.

Page 52, line 19, delete "33" and substitute therefore --44--.

A replacement page 52 is enclosed; a copy of page 52 marked to show the changes is also enclosed.

In the claims

Please cancel claims 1-222, 238-246, and 251-465.

STATEMENT REQUESTING DELETION OF INVENTORS

The declaration that is being filed with the instant application is a copy of the declaration that was filed with U.S. Application Serial No. 08/916,692 filed August 22, 1997. As a result of the restriction requirement in U.S. Application Serial No. 08/916,692, the following inventors named in the grandparent application are not inventors of the invention claimed in the instant divisional application:

Raymond J. Beffa
Frank K. Ross
Larry D. Kinsman
Ronald L. Taylor
John S. Mullin

Please file the instant application in the names of the remaining inventors (Keeth, Bunker and Derner) in accordance with 37 CFR 1.63 (d).

CHANGE OF ADDRESS

Please note that the undersigned attorney's address has changed since the parent application was filed and that the undersigned attorney's address is correctly noted on form PTO/SB/05 filed herewith, and is correctly noted below.

It is respectfully requested that the instant application, covering claims 223-237 and 247-250, receive an early office action on the merits.

Respectfully submitted

Edward L. Pencoske
Reg. No. 29,688
Thorp Reed & Armstrong, LLP
One Oxford Centre
301 Grant Street, 14th Floor
Pittsburgh, PA 15219-1425
(412) 394-7789

Attorneys for Applicants

Dated: 20 June 2001

FIG. 108 is reproduction of FIG. 4f illustrating an array slice to be discussed in connection with the all row high test mode;

FIG. 109 is a reproduction of FIG. 6A with the sense amps and the row decoders illustrated for purposes of explaining the all row high test mode;

FIG. 110 identifies various exemplary dimensions for the chip of the present invention;

FIG. 111 illustrates the bonding connections between the chip and the lead frame;

FIG. 112 illustrates a substrate carrying a plurality of chips constructed according to the teachings of the present invention; and

FIG. 113 illustrates the DRAM of the present invention used in a microprocessor based system.

Microfiche Appendix

Reference is hereby made to an appendix which contains [nine microfiche having a total of fifty-two frames] <u>eleven microfiche having a total of sixty-six frames</u>. The appendix contains [33] <u>44</u> drawings which illustrate substantially the same information as is shown in FIGs. 1-113, but in a more connected format.

FIG. 108 is reproduction of FIG. 4f illustrating an array slice to be discussed in connection with the all row high test mode;

FIG. 109 is a reproduction of FIG. 6A with the sense amps and the row decoders illustrated for purposes of explaining the all row high test mode;

FIG. 110 identifies various exemplary dimensions for the chip of the present invention;

FIG. 111 illustrates the bonding connections between the chip and the lead frame;

FIG. 112 illustrates a substrate carrying a plurality of chips constructed according to the teachings of the present invention; and

FIG. 113 illustrates the DRAM of the present invention used in a microprocessor based system.

Microfiche Appendix

Reference is hereby made to an appendix which contains eleven microfiche having a total of sixty-six frames. The appendix contains 44 drawings which illustrate substantially the same information as is shown in FIGs. 1-113, but in a more connected format.